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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/056,656	04/07/98	PRIEM	C NV30

MF

022903 WM01/0605
COOLEY GODWARD LLP
ATTN: PATENT GROUP
11951 FREEDOM DRIVE, SUITE 1700
ONE FREEDOM SQUARE- RESTON TOWN CENTER
RESTON VA 20190-5061

EXAMINER	
CHAUHAN, U	
ART UNIT	**PAPER NUMBER**
2671	22

DATE MAILED: 06/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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Commissioner of Patents and Trademarks

Ulka J. Chauhan
Primary Examiner
Art Unit: 2671

Office Action Summary	Application No. 09/056,656	Applicant(s) PRIEM ET AL.	
	Examiner Ulka J. Chauhan	Art Unit 2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-89* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-89* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 5/14/01 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/056,656 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 42-61 and 70-81 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claims 42, 51, 70, and 71 recite a On pgs. 11 and 12, the specification discloses that the DMA engine in cooperation with a kernel driver accesses data structures in order to locate texture maps and that an application program provides the addresses of texels needed for the DMA to retrieve the texels into the cache. The specification does not provide any clear written description of a "texture cache controller" or a "cache controller that controls said texture cache memory".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 42-46,48-56, 58-61, 70-75, and 77-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No.5,790,130 to Gannett and U.S. Patent No.6,097,402 to Case et al.

7. As per claims 42 and 44, Gannett teaches a graphics system comprising a host 15 including a main memory 17 and a processor 19, a front end board 10, a texture mapping board 12, and a frame buffer board 14 at Fig. 4. Gannett further teaches that the front end board receives primitives to be rendered from the host computer ("a central processing unit") over bus 16 ("a bus") at col. 12 lines 35-39. Gannett further teaches a texture mapping board 12 that includes texture mapping chip 46, texel cache access circuit 82 comprising four controllers, and cache memory 48 ("a cache controller" and "a texture cache memory") that stores texture MIP map data downloaded from the main memory 17 associated with the primitives being rendered at col. 13 lines 44-55. Gannett also teaches that a texture interrupt managing daemon 160 that replaces cache blocks based on the least recently used blocks and the low priority blocks ("a replacement policy") at col. 42 lines 6-36. And Gannett teaches that texture MIP map data is

downloaded from the main memory through the 2D geometry accelerator to the texture mapping board at col. 13 lines 52-55 and Fig. 4. As per claim 42, Gannett does not expressly teach a DMA engine. Case teaches a computer system comprising a chipset 110 coupled to a memory subsystem 130 and a graphics subsystem 140 wherein a graphics controller of the graphics subsystem operating in a Direct Memory Execute mode, directly operates on texture maps from the memory subsystem at col. 2 lines 43-67 and Fig. 1. Case also teaches a Direct Memory Execute and Local mode of operation in which the graphics controller retrieves frequently used graphics information from the local memory and less frequently used graphics information from the system memory 131 at col. 3 lines 1-8 and Fig. 1. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Gannett and Case such that textures are downloaded using DMA for the purpose of directly transferring the texture data to the cache at a faster rate and without burdening the host CPU.

8. As per claim 43, Gannett teaches that the cache is fully associative at col. 18 lines 57-62.

9. As per claim 45, Gannett teaches a replacement policy based on the priorities of texture map portions at col. 8 lines 22-28. Gannett further teaches that the highest priority is given to textures needed for newly created images and the next highest priority given to the most recently used textures at col. 10 line 64-col. 11 line 4. Therefore Gannett teaches that needed textures have highest priority and are not overwritten.

10. As per claim 46, Gannett teaches that each block of texel data stored in the cache has an associated block tag which is used by the texture interrupt managing daemon 160 for downloading needed blocks at col. 19 lines 4-19.

11. As per claim 48, Gannett teaches that the front end board, texture mapping board, and frame buffer are each pipelined and operate on multiple primitives simultaneously at col. 12 lines 65-67. Gannett teaches that texture data for any primitive is downloaded into the local memory 48 before it is needed by the primitive at col. 42 lines 38-51.

12. As per claim 49, Gannett does not expressly teach that texels are pre-fetched based on whether they can fit into space available in the cache. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have pre-fetched texels into the cache only if there is available space in the cache and otherwise fetch the texels as needed so that texture processing is accelerated by caching texels when possible.

13. As per claim 50, Gannett does not expressly teach that texels are pre-fetched based on whether they fit into ½ of the cache. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have determined if the required texels being pre-fetched for a polygon fit into ½ of the texture cache so that a texels required for the current polygon being processed are not overwritten when the pre-fetching occurs.

14. As per claim 51, Gannett teaches that the when a cache miss occurs the portion of the texture MIP map needed for the primitive is downloaded from the main memory into the cache using the texture interrupt managing daemon 160 at col. 10 lines 44-47 and col. 14 lines 37-44.

15. Claims 52-56, 58-61, 70-75, and 77-81 are similar in scope to claims 42-46 and 48-51, and are rejected under the same rationale.

16. Claims 47, 57, and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,790,130 to Gannett and U.S. Patent No. 6,097,402 to Case et al and U.S. Patent No. 5,926,187 to Kim.

17. As per claims 47, 57, and 76 Gannett does not expressly teach that a DMA engine implements a virtual-physical address translation. Kim teaches a multimedia device 100 including a multimedia processor 200 comprising a DMA controller 255 that provides address translation at col. 2 line 64-col. 3 lines 12, col. 4 lines 26-43, and col. 9 lines 29-31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Gannett, Case, and Kim such that the DMA unit includes address translation for retrieving data using virtual addressing.

18. Claims 62, 63, 65-68, 82-84, 86, 87, and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No.5,790,130 to Gannett and International Publication WO 90/09634 to Olday et al.

19. As per claims 62 and 63, Gannett teaches a graphics system comprising a host 15 including a main memory 17 and a processor 19, a front end board 10, a texture mapping board 12, and a frame buffer board 14 at Fig. 4. Gannett further teaches a texture mapping board 12 that includes texture mapping chip 46 ("a memory control") and cache memory 48 ("memory") that stores texture MIP map data downloaded from the main memory 17 associated with the primitives being rendered at col. 13 lines 44-55. Gannett further teaches that the cache memory stores up to 64 blocks of texture data each including 256x256 texels at col. 32 lines 23-29 and that the texels within the cache are addressed using S and T bits at col. 23 lines 26-38. As per claims 62 and 63, Gannett does not expressly teach an interleaved address with odd numbered bits corresponding to a first dimension coordinate and even numbered bits corresponding to the second dimension coordinates. Olday teaches a memory accessing scheme for accessing memory on a tile basis in which column and row address bits are interleaved such that even bits

of the address define a column address and odd bits define a row address at pg. 6 line 24-pg. 7 line 6 and Figs. 4a and 5. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Gannett and Olday such that the texture cache of Gannett's invention is accessed using the scheme taught by Olday so that data a tile of texture data are accessed for efficient memory access.

20. As per claim 65, Gannett teaches that the cache is fully associative at col. 18 lines 57-62.

21. Claims 66-68, 82-84, 86, 87, and 89 are similar to claims 62, 63, and 65, and are rejected under the same rationale.

22. Claims 64, 69, 85, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,790,130 to Gannett and International Publication WO 90/09634 to Olday et al and U.S. Patent No. 5,945,997 to Zhao et al.

23. As per claims 64, 69, 85, and 88, Gannett does not expressly teach that cache stores texels in cache lines. Zhao teaches texture mapping in a graphics system in which the texture cache 802 stores portions of a texture map on a square by square basis with each square being stored in a cache line 604 and with the entire cache line 604 being replaced with new data when swapping out occurs at col. 14 lines 5-13. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Gannett, Olday, and Zhao so that texture tiles can be easily and efficiently stored and accessed from the texture cache.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art teaches accessing texture data and tiled memory.

U.S. Patent No. 5949429 to Bonneau et al. U.S. Patent No. 6215507 to Nally et al.

U.S. Patent No. 6204863 to Wilde

Igehy, H., Eldridge, M., Proudfoot, K., "Prefetching in a Texture Cache Architecture", Proceedings of the 1998 EUROGRAPHICS/SIGGRAPH Workshop on Graphics Hardware, 1998, pgs. 133-142.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman can be reached on (703) 305-9798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9314.

27. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Ulka J. Chauhan
Primary Examiner
Art Unit 2671

ujc
June 4, 2001